EE / CprE / SE 491 – sdmay20-10
Power Scraping Module
Week 6 Report
11/08/2019 -11/16/2019
Client: Honeywell FM&T
Faculty Advisor: Gary Tuttle

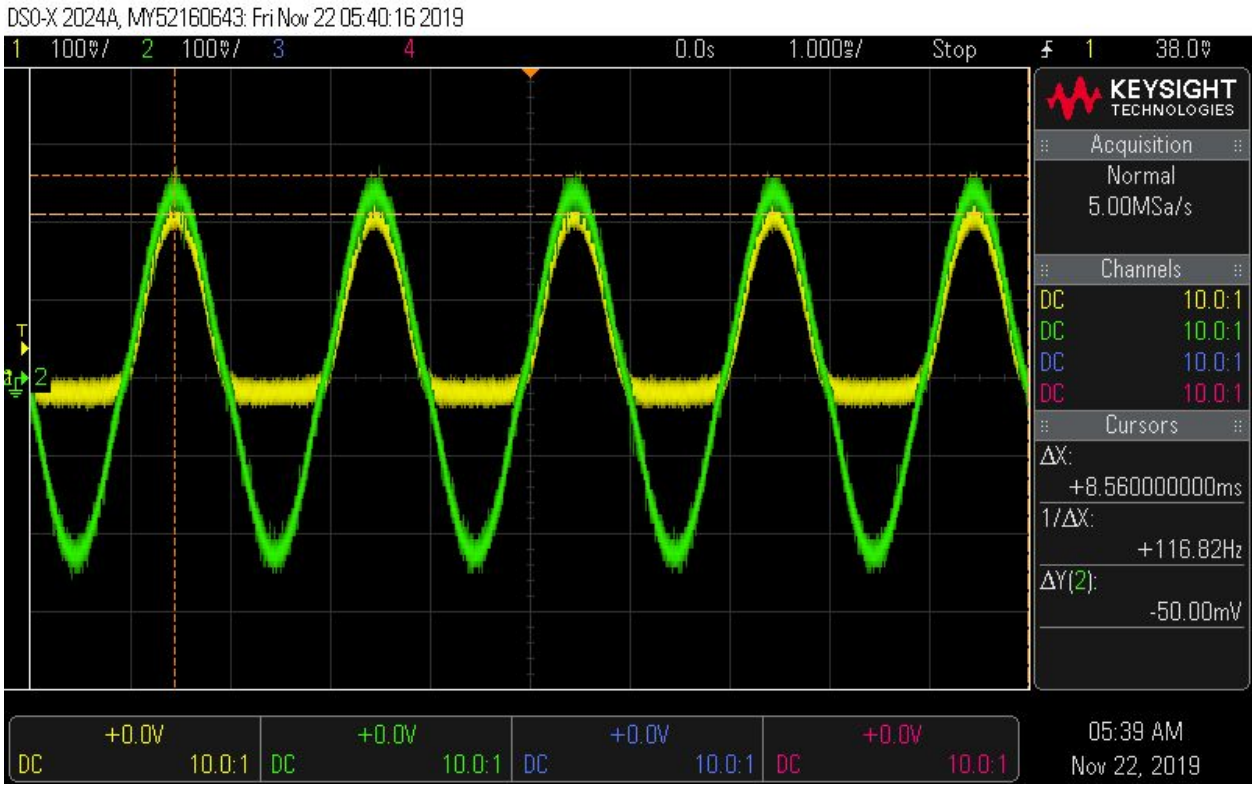
Team Members/Role:

Jordan Fox — Chief Engineer
Xiangyu Cao — Design Engineer
Andesen Ande — Design Engineer
Ahmed Salem — Test Engineer
Ben Yoko — Test Engineer
Shahzaib Shahid — *Team Leader*

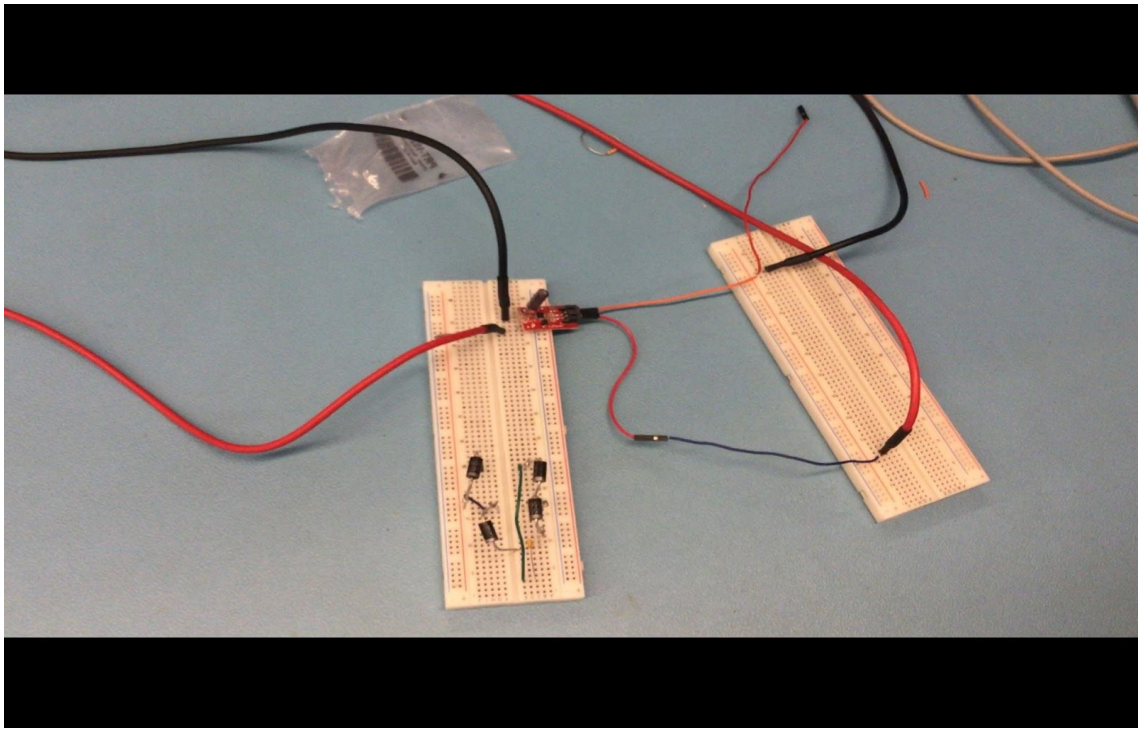
Weekly Summary

This week we continued our testing and made significant progress towards incorporating part of our circuit together. We completed testing the supercapacitor and found precise values that are as expected. We made modifications to our diode testing and received an output we are satisfied with. Lastly, we finally have an indication that the booster we obtained works as intended but there is still some unexpected behavior that is preventing us from implementing and testing. In the meanwhile, we gathered enough documents and images about some challenges in our circuit design to share with our faculty advisor so we can discuss in our next meeting and be capable to incorporate some alternative solutions.

Past Week Accomplishments



The figure above is the output for a full-wave rectifier with .53 V input at 500 Hz. The output behaves precisely as expected, little to no voltage is measured during the negative cycle of the waveform. We were able to determine that the forward voltage drop across was within .2-.3 V which is excellent for our application. After having successfully tested the diode we made the decision to update our design to feature a full wave rectifier instead of a half wave rectifier. Initially we were concerned that the voltage loss would be significant, but the results from this test show that is not the case.



We tested our DC-DC booster with little success. Our setup is shown above, we have the function generator being inputted into the booster module and a multimeter attached to the output of the module. We input a .6 V DC signal and initially saw a voltage output anywhere between 1.5-2V (this was variable each time we tested). This test result demonstrates that the booster works as we expected having a voltage output that is 2-3x larger than the input. However, we observed that the voltage would drop significantly at a fast rate. We still do not have an understanding as to why this occurred. We tried to add different loads to the output of the booster module, but no attempt was successfully at stopping or limiting the voltage drop.

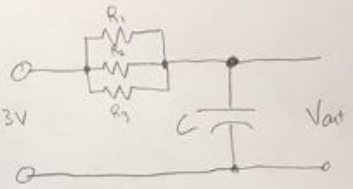
Measured $R_{EQ} = 65\,\Omega$ (calculated = 61.11 Ω)

Input Voltage : 3 VDC

Resistors used : 150, 150, 330 → parallel

63.2% = 1.896 VDC

Time at 1.896 VDC = 62.67 s



$\tau = RC$

$C = \frac{\tau}{R} = \frac{62.67}{65} = 0.964\ F$

Cap 2 : Time to 1.896 VDC = 63.72s

C = 0.98 Farads

Cap 3 : $\tau = 60.1s$, $C = 0.925\ F$

Cap 4 : $\tau = 64.67s$, $C = 0.995\ F$

Cap 5 : $\tau = 64.10s$, $C = 0.986\ F$

Above is our test documentation for each supercapacitor we ordered. In order to test the diodes we created the RC circuit as seen above. Three parallel resistors were placed in series with each supercapacitors being supplied with 3V DC. The time constant of this circuit is approximately 63 percent of the 3V which is 1.89 V. We measured the time it took for the voltage across the capacitor to reach 1.89 V and divided by the measured equivalent resistance of the circuit. All five capacitors were within 10 percent tolerance of the desired 1F. For our application this value does not need to be precise just a relatively high capacitance.

Individual Contributions

Name	**Hours this week**	**Hours Cumulative**
Jordan Fox	6.5	38
Xiangyu Cao	8	40
Andesen Ande	6.5	38
Ahmed Salem	6.5	37.5
Ben Yoko	7.5	40.5
Shahzaib Shahid	7.5	39.5

*Reported times are rough estimates.

Plans for the upcoming week

1. Continue to find a way to test the booster module and understand why the voltage drops at a fast rate.-Shahzaib, Ben, Cao
2. Assemble all components to have a complete breadboard prototype- all team members
3. Finishing completing and revising our design document-- all team members
4. Make progress on our design review presentation- all team members
5. Discuss next semester goals- all team members